Learning to work with SPS Structured Beam

(June 14-21, 2004)

Lev Uvarov

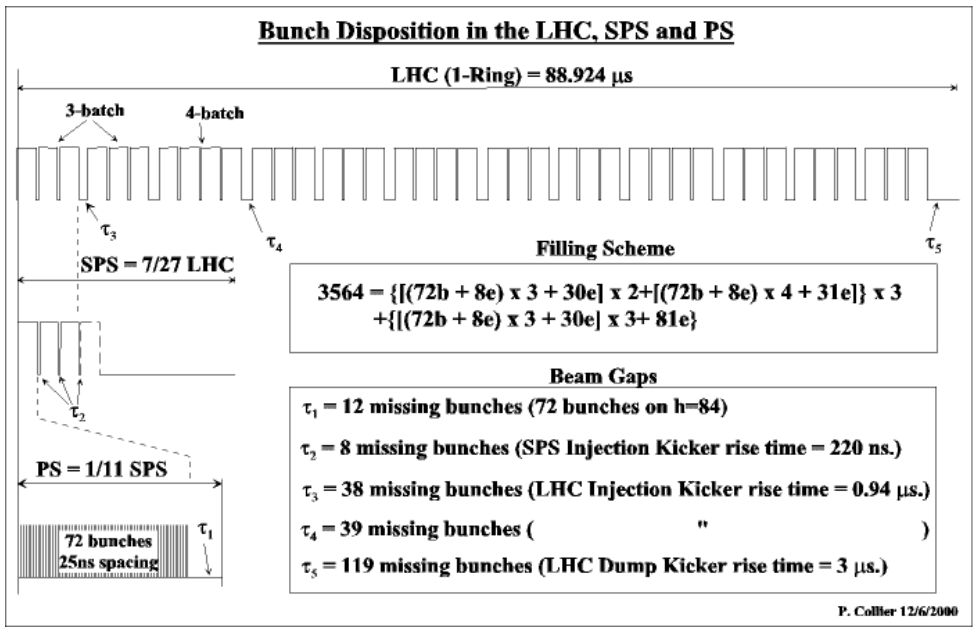
Structured Test Beam at SPS

From Minutes of SPS Users Meeting, Thursday, 17-Jun-2004:

Beam conditions for SPS 25ns run (Monday, June 14, 8:00 - Monday, June 21, 8:00):

- ➔ SPS beam energy 400 GeV/c
- ➔ 1 bunch train of 48 bunches with 25ns spacing (1200 ns length)
- ➔ every 23 *u*s (SPS revolution frequency)
- ➔ spill length 2.2 s
- ➔ cycle length 12.0 s (see details)

… synchronization of the revolution frequency with the 25ns signal … only works at 400 GeV SPS beam:



RF = 24.95 ns

LHC = 3564 * RF = 88.924 us

SPS = 7 / 27 LHC
SPS = 924 * RF = 23.054 us

We expected the Orbit signal to comply with the above formula…
It turned out we were wrong.

SP02 as a BC0 Timing Monitor

The Bunch Counter (BC) is used to monitor the BC0 (Orbit) timing:

- ➔ **BC goes into reset state between spills, when Stop Data Taking or BX Reset is received;**
- ➔ **BC starts incrementing by 1 every RF clock cycle, when a sequence of Start Data Taking and BC0 is received;**
- ➔ **BC runs from 0 to 923;**
- ➔ **Out-of-SYnch (OSY) logic monitors arrival times for all subsequent BC0s;**
- ➔ **The OSY bit is set, if BC0 does not arrive when the BC count is zero;**
- ➔ **The OSY bit is reset, when BX Reset is received (at the end of spill);**
- ➔ **Front panel OSY LED visualizes the OSY bit status;**

Observation:

every single spill the OSY LED goes on. Why?

Guess1. Missing BC0 Timing Marks?

The BC, we are taking about, picks BC0 timing marks from the trigger data path.

Remember,

MPC-to-SP data format specifies two timing marks MPC sends to the SP02:

- **BC0 – a bunch crossing zero mark is sent when the BC value equals zero;**
- **BX0 – a bunch counter least significant bit.**

MPC, in turn, gets data with embedded timing marks from the TMB.

The problem found is:

TMB blanks all the output bits to the MPC when it is not transmitting LCT data frames!

No LCT --> BC0 does not pass through TMB --> SP02 sets the OSY bit

Temporary Solution: Switch BC to the CCB timing.

Observation:

still every single spill the OSY LED goes on. Now why?

Guess2. Is the TTCvi Programmed Correctly?

The problem found is:

All 4 B-Go inputs of the TTCvi are cabled to generate 4 TTC commands:

- ➔ Start Data Taking (0x06)
- ➔ Stop Data Taking (0x07)
- ➔ BX Reset (0x32)
- ➔ BC0 (0x01)

Orbit signal goes into the lowest priority B-Go<3> input.

B-Go<3> transfer mode is set to SINGLE.

In case two or more B-Go signals arrive simultaneously, transfer of the lower priority command may be delayed!

Solution:

rearrange cabling to free up B-Go<0> - the highest priority input.

reprogram B-Go<0> to run into a REPETITIVE mode

Observation 1:

still every single spill the OSY LED goes on. Now why?

Observation 2:

BXN distribution of the SP02 events is about 60bx wide, not 48bx. Why?

Guess3. Is the SPS Orbit Period Stable?

To check this guess an Orbit Analyzer has been built into the SP02 CCB interface firmware.

The Orbit Analyzer measures a number of bunch crossings in every orbit (from a BC0 mark to a subsequent BC0 mark).

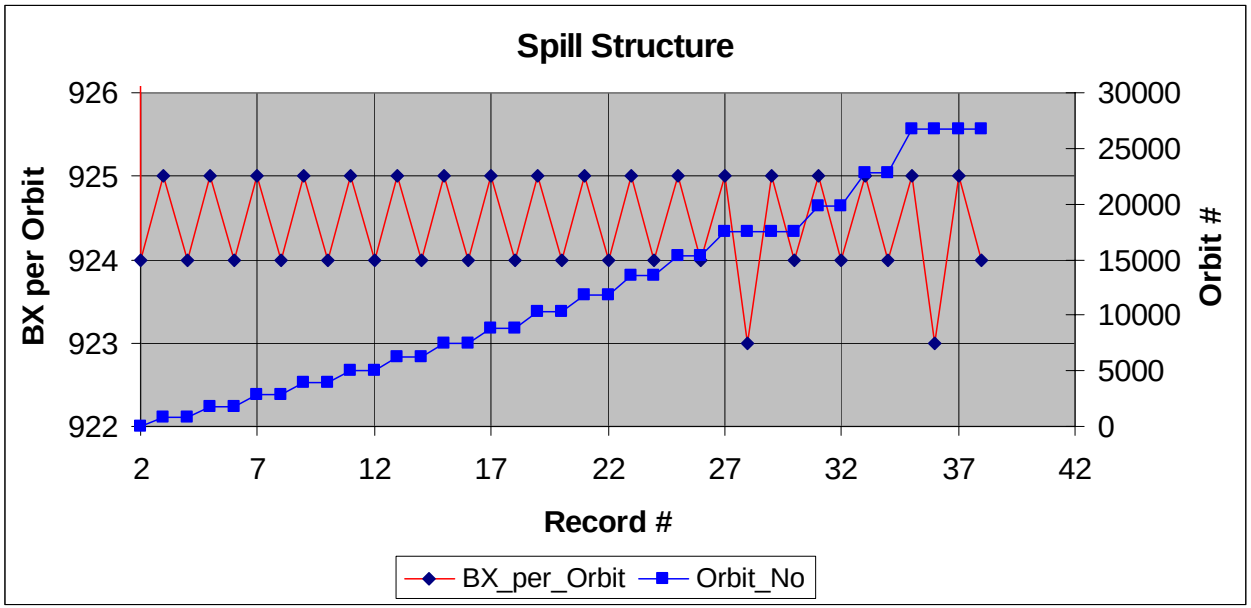
When a change of the orbit period is detected, the Orbit Analyzer records both a new orbit period in bx and the orbit number, when the change occurred.

Here is an example of the Orbit Analyzer log file:

Record_No	Orbit_No	BX_per_Orbit	Comment
1	1	4094	**BC preset value to mark first Orbit in Spill**
2	2	924	**Normal orbit period**
3	769	925	**Orbit with extra bx**
4	770	924	**Normal orbit period**
5	1774	925	**Orbit with extra bx**
6	1775	924	**Normal orbit period**
7	2821	925	**Orbit with extra bx**
8	2822	924	**Normal orbit period**
9	3912	925	**Orbit with extra bx**
10	3913	924	**Normal orbit period**

Spill structure

Plot below shows a single spill structure and looks like a ladder with narrow and wide steps.
Record 1 is omitted, since it serves only as a begin-of-spill mark.
Each narrow step represents two successive orbits:
a 925bx orbit period immediately reverts to a 924bx orbit period.
Each wide step represents four successive orbits, orbit period oscillates:
925bx -> 923bx -> 925bx -> 924bx.



Spill Structure continue

Plots below show:

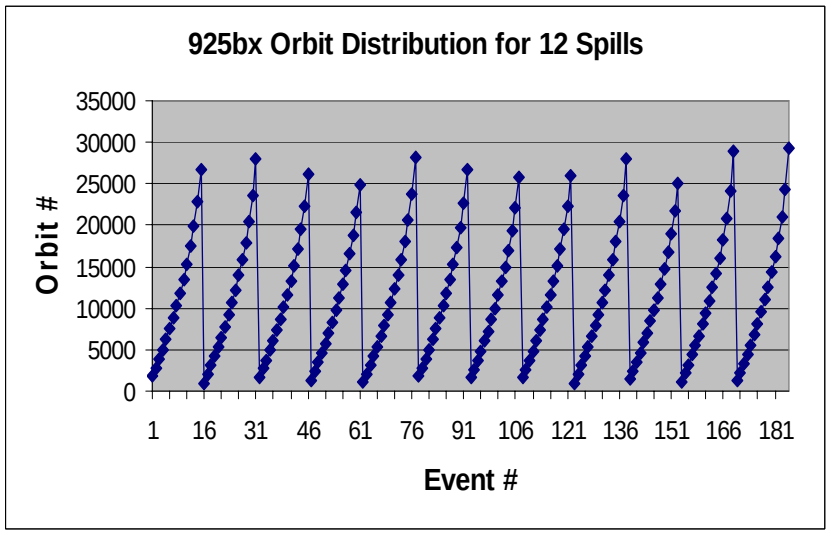
- ➔ **Distribution of orbit disturbances versus orbit # (versus time!)**
- ➔ **Distribution of orbits elapsed since previous orbit disturbance versus orbit number (versus time!), superimposed for 12 spills.**

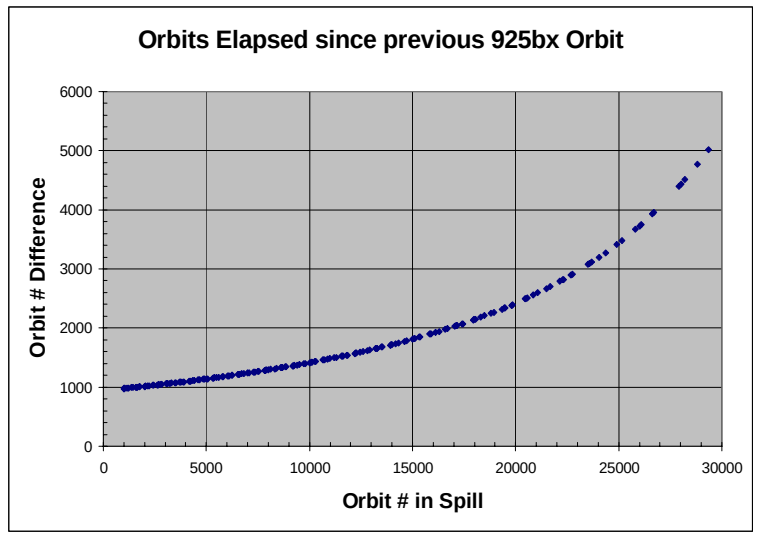
Only first orbit of the "ladder step" is plotted
(remember, a disturbance always begins with a 925bx orbit).

Conclusion:

Orbit disturbances occur 15-16 times during first 0.7 sec (23 us * 30000) of spill.

If BC is synchronized to BC0 only at the beginning of spill, it will be apart from BC0 by 15-16bx to the end of spill -> BXN distribution of the events gets wider.





Conclusion

Solution:

Use BC0 as a BC Reset

The SP02 firmware is modified accordingly.
Every BC0 now resets the BC,
so the BC always runs under control of the orbit signal.

Observation 1:

BXN distribution of the events is exactly 48 bx wide → very good!

Observation 2:

It looks like beam extraction phase begins at a slightly lower than nominal revolution frequency (needed 15-16 extra bx to compensate).

Observation 3:

Nevertheless, SP02 needs BC0 timing marks (link "heartbeat"!) on every link regardless of LCT presence to maintain proper timing in Front FPGAs (a separate presentation may require to explain it in detail) .

LHC Structured Test Beam in May 2000 (from Bruce Taylor Presentation on Timing WG Meeting July 14, 2000)